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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,398	06/01/2001	Micha Risling	N-95-7 US	2871

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2132	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,398	RISLING ET AL.	
	Examiner	Art Unit	
	Venkatanarayanan Perungavoor	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specifications

On Page 5 and Page 6 under the *Brief Description of The Drawings* of the Specifications the Applicant mentions Figure 4 and Figure 5 two times.

Appropriate correction is required.

Claim Rejections – 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4410990 to Wilkinson

3. Regarding Claim 1, The "initializing scrambling step comprising the steps of generating a scrambling bit sequence and storing said scrambling bit sequence in a scrambling register **[see Column 2 Line 22-28]**

and said subsequent scrambling step comprising storing a sequential group of bits in the same sequence in which they were received , each of said group of bits containing the same number or fewer bits than said scrambling bit sequence, **[see Column 1 Line 67-Column 2 Line 5]**

XOR-ing said sequential group of bits with corresponding bits of said scrambling bit sequence in parallel, thereby generating scrambled bits;

shifting said bits in said scrambling register by a number of spaces equal to the number of scrambled bits and subsequently transmitting and storing said scrambled bits in corresponding cells of said scrambling register in lowest ordinal sequence for use in subsequent XoR-ing of a next sequential group of bits" [**see Abstract & Column 1 Line 44- Column 2 Line 36].**

4. Claim 4, 7, 10 are rejected under the same rationale as Claim 1 above.

5. Regarding Claim 13,

- a source of serially transmitted bits(**see Column 2 Line 21-25**)
- an input register comprising a first number of cells for storing a sequence of bits in the same sequence in which they were received(**see Figure 2 item 8**)
- a scrambling register comprising at least a second number of cells, said second number being higher than the number of bits in said received group, for storing at least said second number of scrambling bits, wherein initially a second number of bits is loaded into said scrambling register, and subsequently each scrambling bit is a scrambled bit preceding the bit to be scrambled by it, by said second number (**see Figure 2 item 10-13)**
- a first number of XOR gates for the parallel scrambling of said first number of input bits, having two inputs and one output each, wherein, one XOR gate input is correspondingly connected to a cell in said first register, second XOR gate input is correspondingly connected to a cell in said scrambling register, said one XOR gate output is stored for corresponding sequential transmission to a

receiver, stored for subsequent use in said scrambling register for scrambling next input bit separated from said input bit by said second number of bits**(see Figure 2 item 5 and item 20).**

- clock means operatively connected for the enabling and the disabling of data handling operations **(see Figure 2 item 7).**

6. Claim 16 is rejected under the same rationale as Claim 13 above.

7. Regarding Claim 21, The "one input for each XOR operation is a descrambled bit descrambled bits, in a sequence of a second input for each XOR operation is a scrambled bit of said sequence, preceding said descrambled bit by forty three bits**(see Figure 2 item 4 and item 6).**

- the output of each one of said XOR operation is a scrambled bit in a sequence of scrambled bits**(see Figure 2 item 3).**

8. Regarding Claim 22, The "one input for each XOR operation is a scrambled bit in a sequence of scrambled bits, a second input for each XOR operation is a scrambled bit of said sequence, preceding said scrambled bit by forty three bits**(see Figure 2 item 20 and item 19).**

- the output of each one of said XOR operation is an descrambled bit in a sequence of descrambled bits **(see Figure 2 item 22).**

Claim Rejection – 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4410990 to Wilkinson. in view of U.S. Patent No. 5459723 to Thor

11. Regarding Claim 3, Wilkinson discloses the use of 15 bits being processed in parallel **see Column 3 Line 35-53.** However, Thor discloses 32 bits being used for HDLC transmitter **Column 10 Line 67- Column 11 Line 6**. It would be obvious to one having ordinary skill in the art at the time of the invention to modify the instant invention from 15 bits being processed in parallel to 32 bits being processed in parallel in order for it to be adaptable for HDLC transmitter **Column 10 Line 67- Column 11 Line 6.**

12. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4410990 Wilkinson. in view of U.S. Patent No. 62690961 B1 to Hann et al.

13. Regarding Claim 2, Wilkinson discloses the use of scrambling bit sequence comprised of forty five bits **see Column 2 Line 61-64.** However, Hann et al. discloses the use of forty three bits **see Column 6 Line 57-60.** It would be

obvious to one having ordinary skill in the art at the time of the invention to modify the scrambling bit sequence comprised of forty five bits to forty three bits in order to adaptable to ATM standards **see Column 6 Line 53-55.**

14. Claim 5, 8, 11,15,18, 20 are rejected under the same rationale as Claim 2 above.

15. Claim 6, 9,12, 14,17,19 are rejected under the same rationale as Claim 3 above.

Conclusion

16. The following patents are cited to further show the state of art in general:

U.S. Patent No. 4827513 to Austin

U.S. Patent No. 5007088 to Ooi et al.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Venkatanarayanan Perungavoor whose telephone number is 571-272-7213. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Venkatanarayanan Perungavoor
Examiner
Art Unit 2132

VP
2/3/05

GILBERTO BARRON JR.
SUPERVISORY PATENT EXAMINER
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